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whereby the gate of the first transistor and the gate of the third transistor are coupled together to a DC voltage.

Please add the following new claim:

17. (New) The pixel as recited in Claim 13, wherein said gate of said first transistor is at a first voltage and said first electrode of said first transistor is at a second voltage, said second electrode of said first transistor being connected to said photosensitive element.

REMARKS

The Examiner rejected claims 13-15 under 35 U.S.C. § 102(b) as being anticipated by Miyatake. The Examiner rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Miyatake.

The Examiner has taken the position that Miyatake discloses a pixel for imaging applications fabricated in MOS technology, the pixel comprising: a photosensitive element and a first transistor having a gate and a first and second electrode and being in series with the photosensitive element, the first transistor and the photosensitive element forming a first connection; a second transistor having a gate, the second transistor being coupled to the first connection forming a second connection, the second transistor being part of an amplifying circuit; and a third transistor having a gate and having two electrodes, the third transistor being connected in the second connection between the first connection and the second transistor; whereby the gate of the first transistor and the gate of the third transistor are coupled together. Applicants have amended claim 13 to include the limitation of claim 17 that the gate of the first and third transistors are coupled to a DC voltage.

Claim 13 has been amended to incorporate the limitation of claim 16. From a quick comparison of claim 13 and the pixel of Figure 6 of Miyatake, one can readily see that present claim 13 is not obvious. In Miyatake, not only the gates of the first and third transistor are connected to each other, but also the gate of the second transistor. Therefore, if the gates of the first and third transistor in the Miyatake pixel are coupled together to a DC voltage, then a constant voltage (the applied DC voltage) is also applied to the gate of the third transistor (2(b) in Figure 6 of Miyatake). If such a constant voltage were applied to the gate of the second transistor of the Miyatake pixel, the signal collected on the photosensitive element would not be transferred for amplification – the signal would be effectively short-circuited. Also, on applying such a DC voltage to the gate of the first and third transistors in the Miyatake pixel, these

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transistors would not be, contrary to what is stated by the Examiner, "properly biased to obtain a desired result." Rather, the pixel would cease to function and would not produce an output signal related to charges collected on the photosensitive element at all. In other words, the desired result would not be obtained because of the fact that the gate of the second transistor is also coupled to the gate of the first and third transistors. Accordingly, one of ordinary skill in the art would not modify the pixel of Miyatake as suggested by the examiner.

Unlike Miyatake with the modification suggested by the Examiner, in the pixel of the present claims, with the gates of the first and third transistors coupled together to a DC voltage, the pixel functions as a pixel and delivers at its output a signal which is related to the charges collected by the photosensitive element.

In view of the above remarks, amended claim 13 is novel and non-obvious over Miyatake. In addition, claims 14-15 and new claim 17, which depend on claim 13, are also patentable. Accordingly, all claims are believed to be in the condition for allowance, and allowance is earnestly solicited. Should any issues remain to be resolved, the Examiner is invited to contact the undersigned such that the case may be passed quickly to issuance.

Attached hereto is a marked-up version of the changes made to the specification and claim 13 by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: ~~May~~ June 1, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

13. (Amended) A pixel for imaging applications fabricated in a MOS technology, said pixel comprising:

a photosensitive element and a first transistor having a gate and a first and second electrode and being in series with said photosensitive element, said first transistor and said photosensitive element thereby forming a first connection;

a second transistor having a gate, said second transistor being coupled to said first connection, thereby forming a second connection, and said second transistor being part of an amplifying circuit; and

a third transistor having a gate and having two electrodes, said third transistor being connected in said second connection between said first connection and said second transistor;

whereby the gate of the first transistor and the gate of the third transistor are coupled together to a DC voltage.

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